What is claimed is:

1. A tri-level decoder circuit comprising:

a first decoder circuit that is coupled between an input node and a first output node, wherein the first decoder circuit includes:

a first switch circuit that is coupled to the input node; and

a first current mirror circuit that is coupled between the first switch circuit and the first output node; and

a second decoder circuit that is coupled between the input node and a second output node.

2. The tri-level decoder circuit of Claim 1, wherein

the first current mirror circuit is configured to:

receive a first switch current from the first switch circuit; and

reflect the first switch current to provide a first reflected current at the first output node in accordance with a ratio that is greater than one-to-one.

3. The tri-level decoder circuit of Claim 1,

wherein the first decoder circuit further includes a first current source circuit coupled to the first switch circuit, and

wherein the first switch circuit is configured to:

if a control voltage exceeds a low threshold, reduce a resistance between a first port of the first current mirror circuit and the first current source; else

isolate the first port of the first current mirror circuit from the first current source.

4. The tri-level decoder circuit of Claim 3, wherein

the first current source circuit comprises at least one of a transistor and a resistor.

5. The tri-level decoder circuit of Claim 3, wherein

the first decoder circuit further includes another current source circuit coupled to the first output node.

6. The tri-level decoder circuit of Claim 5,

wherein the first decoder circuit further comprises:

a first current branch including the first current source circuit and the first switch circuit; and

a second current branch including the other current source and the output node, and

wherein the first current mirror circuit includes at least one component in each of the first and second current branches.

7. The tri-level decoder circuit of Claim 1, further comprising:

a driver circuit that is coupled to a control node associated with the input node, wherein the driver circuit is configured such that

if the input node does not receive a driving input signal, the driver circuit actively drives the control node.

8. The tri-level decoder circuit of Claim 7, wherein

the driver circuit comprises two current sources and two transistors, wherein each of the two transistors is configured to operate as a diode.

9. The tri-level decoder circuit of Claim 7, further comprising:

a low-pass filter circuit that is coupled between the control node and the input node.

10. The tri-level decoder circuit of Claim 9, wherein the low-pass filter circuit comprises:

a resistor that is coupled to the driver circuit;

a capacitor that is coupled between the resistor and a first bias node,

wherein the first decoder circuit further includes a first current source circuit coupled to the first switch circuit and the first bias node; and

another resistor that is coupled between the input node and the resistor.

11. The tri-level decoder circuit of Claim 1, wherein

the second decoder circuit includes:

a second switch circuit coupled to the input node;

a second current source circuit coupled to the second switch circuit; and

a second current mirror circuit coupled between the second switch circuit and the second output node.

12. The tri-level decoder circuit of Claim 11, further comprising:

a capacitor that is coupled between the second output node and another node between the second current mirror and the second switch circuit.

13. The tri-level decoder circuit of Claim 1, wherein

the first decoder circuit further comprises a non-linear filter circuit.

14. The tri-level decoder circuit of Claim 13, wherein

the non-linear filter circuit comprises a capacitor.

15. The tri-level decoder circuit of Claim 14, wherein

the capacitor is coupled between the first output node and another node between the first switch circuit and the first current mirror circuit.

16. The tri-level decoder circuit of Claim 14, wherein

the capacitor has a capacitance that is less than .5 picofarads.

17. A tri-level decoder circuit, comprising:

a first switch circuit that is coupled to a first switch node, a first mirror node, and a control node, wherein

the first switch circuit is configured to:

receive a control voltage at the control node;

reduce a resistance between the first mirror node and the first switch node if the control voltage exceeds a low threshold; else

isolate the first mirror node from the first switch node; and

a first current source circuit that is coupled to the first switch node;

a first current mirror circuit that is coupled to the first mirror node and a first output node, wherein

the first current mirror circuit is configured to:

receive a first switch current at the first mirror node; and

reflect the first switch current to provide a first reflected current at the first output node according to a pre-determined ratio that is greater than one-to-one;

a second current source circuit that is coupled to the first output node;

a second switch circuit that is coupled to a second switch node, a second mirror node, and a control node, wherein

the second switch circuit is configured to:

receive the control voltage;

if the control voltage exceeds a high threshold, isolate the second mirror node from the second switch node; else

reduce a resistance between the second mirror node and the second switch node; and

a third current source circuit that is coupled to the second switch node;

a second current mirror circuit that is coupled to the second mirror node and a second output node, wherein

the second current mirror circuit is configured to:

receive a second switch current at the second mirror node; and

reflect the second switch current to provide a second reflected current at the second output node according to another pre-determined ratio that is greater than one-to-one; and

a fourth current source circuit that is coupled to the second output node.

18. The tri-level decoder circuit as in Claim 17, further comprising:

a capacitor that is coupled between that first mirror node and the first output node; and

another capacitor that is coupled between that second mirror node and the second output node.

19. The tri-level decoder circuit as in Claim 17, further comprising:

a modified wilson current mirror circuit that is coupled to a first bias node and a second bias node,

wherein the first current source circuit comprises a first current source transistor having a gate that is coupled to the first bias node,

the second current circuit comprises a second current source transistor having a gate that is coupled to the first bias node,

the third current source circuit comprises a third current source transistor having a gate that is coupled to the second bias node, and

the fourth current circuit comprises a fourth current source transistor having a gate that is coupled to the second bias node.

20. A tri-level decoder circuit, comprising:

means for comparing a voltage to a first threshold;

means for comparing the voltage to a second threshold;

means for providing a current in response to the first threshold comparison; and

means for reflecting the current to provide another current.